have been withdrawn from consideration, but may be reconsidered upon allowance of a generic claim under 37 CFR § 1.141. New claims 21-42 have been added.

In the final office action, claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,471,373 to Shimizu et al. (Shimizu). Claims 3-9 and 13-14 were rejected under 35 U.S.C. § 103(a) as being obvious over Shimizu. Applicant respectfully traverses these rejections.

The action alleges that Shimizu discloses all the features of a semiconductor integrated circuit device recited in claims 1 and 2 relying on Shimizu Figures 1-3 and 18 and a semiconductor substrate (10), transistors Q1, Q2, QE1, QE2, QE3, including gate insulation films of different thicknesses, a terminal for external connection 5 formed on the substrate, and a transistor QE2 allegedly directly connected to the terminal 5 and being a transistor other than the transistor having the thinnest gate insulation film.

As amended, claim 1 recites that a transistor physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

The final office action alleges that the transistor QE2 (in FIG. 18 of Shimizu) which is to be connected to terminal 5 (in FIG. 1 of Shimizu) shows a transistor connected directly to the input/output terminal as recited in the claim 1 invention. According to FIG. 18 and the corresponding description at column 6, line 66 to column 7, line 10 of Shimizu, the transistor QE2 is used for the writing operation, and is connected with an interconnection layer 31. There is no

teaching or suggestion that the transistor QE2 is *physically connected* to terminal 5 (in FIG. 1). For at least these reasons, Shimizu lacks a teaching of all the features recited in claims 1 and 2. Claims 3-9, 13 and 14, which ultimately depend from claim 1 are patentably distinct for the same reasons as claim 1, and further in view of the additional advantageous features recited therein.

New independent claims 21 and 32 are also patentably distinct from the art of record including Shimizu. For example, Shimizu is totally silent as to an input/ouput terminal formed on the semiconductor substrate, wherein a transistor connected directly to the input/output terminal, *absent any intervening elements*, is one of the transistors other than a transistor having the thinnest gate insulation film as recited in claim 21. Similarly, Shimizu is totally devoid of a teaching directed to an input/ouput terminal formed on the semiconductor substrate, wherein a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Claims 22-31, which ultimately depend from claim 21, and claims 33-42, which ultimately depend from claim 32, are allowable for the same reasons as their ultimate base claim, and further in view of the additional advantageous features recited therein.

CONCLUSION

In light of the foregoing, applicant respectfully submits that the instant application is in condition for allowance, and solicits prompt notification of the same.

Respectfully submitted,

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